

(SYLLABUS)

1.

(Course Title)		(Instructor)			
(Year)	2024	(Semester)	2	(Course No.)	2150418101
(Class)	01	(Open to)	3 IT ( ),	(Course Classification)	-IT / -
/	3.0 (1 ) / 3		100	가	가
(Office)	10704	(Telephone)	02-828-7489	(e-mail)	inchul.song@ssu.ac.kr
	(FL), (PBL)		+		2023
	(*) (ABEEK Classification)			(*) (ABEEK Requirement)	
	(C),				
(Course Description)	Top-down HDL , Counter, Shifter Subsystem				

Verilog HDL	
	IT

가	( 100 )	( 100%)
	100	100

## (SYLLABUS)

(Required Texts)		* /Digital System Designs and Practices////Ming-Bo Lin/Wiley/2008/
	( )	* /Modeling, synthesis, and rapid prototyping with the Verilog HDL/M Ciletti/Prentice-Hall/1999/ * /HDL SOC IP / / /2004/ * / LMS/2023
	:	(C)
	- Engaged learning . - . , - : / 50%, 15%, 25%, 10%	

2.

(Week)	(Keyword)	(Description)		(Texts)
01		HDL		,
02	Verilog HDL	Verilog HDL syntax.		,
03	Dataflow	continuous assignment		, ( )
04	Dataflow		, , ,	,
05	Simulation	Verilog HDL S/W , simulation , Testbench	,	,
06	Behavioral	Behavioral H/W	,	,
07	Behavioral	Behavioral ,	,	,
08	Behavioral	Behavioral .	, ,	,
09		: microprocessor/FIR filter .	, ,	,
10	FSM	Finite state machine - state diagram, :	, , , , , ,	,
11	FSM	Finite state machine - ASM chart, :	, , , , , ,	,
12		( / )		/
13	, task	VerilogHDL task, :	, ,	,
14	RTL(Register Transfer Level)	RTL(Register Transistor Level) ,	, ,	,
15	Design example	Design example: sequential logic,	, ,	,

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3. ( )

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	Open-ended problem		
	Teamwork		
	Communication skills		